WHAT IS CLAIMED IS:

1. A power MOSFET device comprising:

a low resistance substrate of the first conductivity type;

a high resistance epitaxial layer of the first conductivity type formed on the low resistance substrate;

a base layer of the second conductivity type formed in a surface region of said high resistance epitaxial layer;

a source region of the first conductivity type formed in a surface region of the base layer;

a gate insulating film formed on the surface of said base layer so as to contact said source region;

a gate electrode formed on said gate insulating film; and

an LDD layer of the first conductivity type formed on the surface of said high resistance epitaxial layer oppositely relative to said source region and said gate electrode;

wherein said LDD layer and said low resistance substrate are connected to each other by said high resistance epitaxial layer.

2. The device according to claim 1, wherein said LDD layer has a bottom section formed at a level shallower than said base layer.

3. The device according to claim 1, wherein

said LDD layer has a bottom section formed at a level deeper than said base layer.

4. The device according to claim 1, further comprising:

a low resistance intermediate layer of the first conductivity type formed in a lateral section of said base layer facing said LDD layer and a region of said epitaxial layer held in contact with said LDD layer and having an impurity density higher than said epitaxial layer.

5. The device according to claim 1, further comprising:

a current conducting layer formed in said epitaxial layer to directly continue from said LDD layer so as to project toward said low resistance substrate.

6. The device according to claim 1, wherein the bottom of said base layer is held in contact with said low resistance substrate.

7. The device according to claim 1, wherein said LDD layer is formed in a self-aligning manner by using said gate electrode as mask.

8. The device according to claim 2, wherein said LDD layer is formed in a self-aligning manner by using said gate electrode as mask.

9. The device according to claim 3, wherein said LDD layer is formed in a self-aligning manner

by using said gate electrode as mask.

10. The device according to claim 4, wherein said LDD layer is formed in a self-aligning manner by using said gate electrode as mask.

11. The device according to claim 5, wherein said LDD layer is formed in a self-aligning manner by using said gate electrode as mask.

12. The device according to claim 6, wherein said LDD layer is formed in a self-aligning manner by using said gate electrode as mask.

13. The device according to claim 1, further comprising:

an extension layer of the second conductivity type formed in a lateral section of said base layer facing said LDD layer and a surface region of said epitaxial layer and at least held in contact with said LDD layer, said extension layer having an impurity concentration lower than that of said base layer.

14. The device according to claim 13, wherein said extension layer of the second conductivity type is formed in said epitaxial layer so as to cover the periphery of said base layer.

15. The device according to claim 13, wherein said extension layer of the second conductivity type is formed in said epitaxial layer between said base layer and said LDD layer.

16. The device according to claim 15, wherein

said extension layer of the second conductivity type is formed in said epitaxial layer so as to cover the periphery of said base layer.

17. The device according to claim 13, wherein the bottom of said base layer is held in contact with said low resistance substrate.

18. The device according to claim 14, wherein the bottom of said base layer is held in contact with said low resistance substrate.

19. The device according to claim 15, wherein the bottom of said base layer is held in contact with said low resistance substrate.

20. The device according to claim 17, wherein said LDD layer is formed in a self-aligning manner by using said gate electrode as a mask.

21. The device according to claim 1, wherein said LDD layer has a length between about 0.7 μm and about 0.8 μm.

22. The device according to claim 13, wherein said LDD layer has a length between about 0.7 μm and about 0.8 μm.

23. The device according to claim 21, wherein the dose of said LDD layer is not higher than $6.0 \times 10^{11}/cm^2$.

24. The device according to claim 22, wherein the dose of said LDD layer is not higher than $6.0 \times 10^{11}/cm^2$.

25. A power MOSFET device comprising:

a low resistance substrate of the first conductivity type;

a high resistance epitaxial layer of the first conductivity type formed on the low resistance substrate;

a base layer of the second conductivity type formed in a surface region of said high resistance epitaxial layer;

a source region of the first conductivity type formed in a surface region of the base layer;

an LDD layer of the first conductivity type formed in a surface region of said high resistance epitaxial layer at a position separated from said base layer by a predetermined distance;

a gate insulating film formed to bridge said source region and an end of said LDD layer;

a gate electrode formed on said gate insulating film;

a sinker layer of the first conductivity type formed between the other end of said LDD layer and said low resistance substrate; and

an extension layer of the second conductivity type formed between the lateral side of said base layer facing said LDD layer and said LDD layer and being at least held in contact with said base layer.

26. The device according to claim 25, wherein

said sinker layer is a dopant diffusion layer of the first conductivity type.

27. The device according to claim 25, wherein said sinker layer has a trench formed so as to extend from said LDD layer to said low resistance substrate, a low resistance layer of the first conductivity type formed on a lateral surface of said trench and an insulating film buried in said trench.

28. The device according to claim 25, wherein said sinker layer has a trench formed so as extend from said LDD layer to said low resistance substrate and a low resistance semiconductor layer of the first conductivity type buried in said trench.

29. The device according to claim 25, wherein said sinker layer has a trench formed so as extend from said LDD layer to said low resistance substrate and a metal layer buried in said trench.

30. The device according to claim 25, wherein said extension layer of the second conductivity type is formed so as to extend to said sinker layer and cover the periphery of said base layer.

31. The device according to claim 26, wherein said extension layer of the second conductivity type is formed so as to extend to said sinker layer and cover the periphery of said base layer.

32. The device according to claim 27, wherein said extension layer of the second conductivity

type is formed so as to extend to said sinker layer and cover the periphery of said base layer.

33. The device according to claim 28, wherein said extension layer of the second conductivity type is formed so as to extend to said sinker layer and cover the periphery of said base layer.

34. The device according to claim 29, wherein said extension layer of the second conductivity type is formed so as to extend to said sinker layer and cover the periphery of said base layer.

35. The device according to claim 30, wherein said extension layer of the second conductivity type is formed in said epitaxial layer so as to bridge said base layer and said LDD layer.

36. The device according to claim 30, further comprising:

an auxiliary current conducing layer of the first conductivity type formed between said LDD layer and said sinker layer.

37. The device according to claim 25, wherein the bottom of said base layer is held in contact with said low resistance substrate.

38. The device according to claim 26, wherein the bottom of said base layer is held in contact with said low resistance substrate.

39. The device according to claim 27, wherein the bottom of said base layer is held in contact

with said low resistance substrate.

40. The device according to claim 28, wherein the bottom of said base layer is held in contact with said low resistance substrate.

41. The device according to claim 29, wherein the bottom of said base layer is held in contact with said low resistance substrate.

42. The device according to claim 36, wherein said LDD layer is formed in a self-aligning manner by using said gate electrode as a mask.

43. The device according to claim 37, wherein said LDD layer is formed in a self-aligning manner by using said gate electrode as a mask.

44. A power MOSFET device comprising:

a low resistance substrate of the first conductivity type;

a high resistance epitaxial layer of the second conductivity type formed on the low resistance substrate;

a base layer of the second conductivity type formed in a surface region of said high resistance epitaxial layer;

a source region of the first conductivity type formed in a surface region of the base layer;

an LDD layer of the first conductivity type formed in a surface region of said high resistance epitaxial layer at a position separated from said base layer by a

predetermined distance;

a gate insulating film formed to bridge said source region and an end of said LDD layer;

a gate electrode formed on said gate insulating film; and

a sinker layer of the first conductivity type formed between the other end of said LDD layer and said low resistance substrate.

45. The device according to claim 44, wherein the bottom of said base layer is held in contact with said low resistance substrate.

46. The device according to claim 44, further comprising:

an auxiliary current conducing layer of the first conductivity type formed between said LDD layer and said sinker layer.

47. The device according to claim 45, further comprising:

an auxiliary current conducing layer of the first conductivity type formed between said LDD layer and said sinker layer.